

B: Amendments to The Claims:

What is claimed is:

1. (Cancelled by this amendment)

1 Claim 2. (Currently Amended) An apparatus comprising:
2 a processor handling an I/O request in an I/O operation;
3 main storage controlled by the processor for storing data;
4 one or more I/O devices for sending data to or receiving data from said main
5 storage;
6 a vector mechanism operable to register I/O requests by said devices to send or
7 receive data from said main storage;
8 a dispatcher operable to poll said vector mechanism to determine if there is an
9 outstanding I/O request; and
10 an override bit having a first condition when an immediate interrupt is to be sent to
11 said processor for handling an I/O request from said I/O device(s), and a second condition
12 when said dispatcher is to poll said vector mechanism to determine if there is an
13 outstanding I/O request, said override bit being set to its first condition or reset to its
14 second condition by said processor, and
15 ~~The apparatus of claim 1~~ further comprising a Target Delay Interval (TDI) register
16 containing a TDI value for determining when the vector mechanism should not be polled
17 by said dispatcher and an interrupt given to said processor, and wherein said ~~override~~
18 override bit, when in its first condition, ~~overrides~~ overrides said TDI value and drives an
19 immediate interrupt to said processor.

1 Claim 3. (Currently Amended) The apparatus of claim ~~1~~ 2 wherein
2 said main storage is divided into multiple partitions, with each partition having a vector
3 mechanism operable to register I/O requests by said devices to send or receive data from
4 that partition of main storage, each partition having an associated override bit for that
5 partition, and said processor is a hypervisor for setting the override bit for that partition



6 when said hypervisor is to handle an immediate interrupt rather than polling by said
dispatcher for that partition.

1 Claim 4. (Original). The apparatus of claim 3 further comprising one or more
2 central processing units (CPUs) assignable by said hypervisor to one or more of said
3 partitions, said hypervisor further setting the override bit of one partition when that
4 partition does not have a CPU assigned to it.

Claim 5. (Cancelled by this amendment)

Claim 6. (Cancelled by this amendment)

Claim 7. (Cancelled by this amendment)

1 Claim 8. (Currently Amended) An apparatus controlling the transfer of data
2 in a data processing system having a processor handling an I/O request in an I/O operation,
3 main storage controlled by the processor for storing data, and one or more I/O devices for
4 sending data to or receiving data from said main storage, said apparatus comprising:
5 a vector mechanism operable to register I/O requests by said devices to send or
6 receive data from said main storage;
7 a dispatcher operable to poll said vector mechanism to determine if there is an
8 outstanding I/O request;
9 an override bit having a first condition when an immediate interrupt is to be sent to
10 said processor for handling an I/O request from said I/O device(s), and a second condition
11 when said dispatcher is to poll said vector mechanism to determine if there is an
12 outstanding I/O request, said override bit being set to its first condition or reset to its
13 second condition by said processor, and
14 ~~The apparatus of claim 7~~ further comprising a Target Delay Interval (TDI) register
15 containing a TDI value for determining when the vector mechanism should not be polled
16 by said dispatcher and an interrupt given to said processor, and wherein said ~~override~~



17 override bit, when in its first condition, ~~overrides~~ overrides said TDI value and drives an
18 immediate interrupt to said processor.

1 Claim 9. (Currently Amended) The apparatus of claim 7 8-wherein said main
2 storage is divided into multiple partitions, with each partition having a vector mechanism
3 operable to register I/O requests by said devices to send or receive data from that partition
4 of main storage, each partition having an associated override bit for that partition, and said
5 processor is a hypervisor for setting the override bit for that partition when said hypervisor
5 is to handle an immediate interrupt rather than polling by said dispatcher for that partition.

1 Claim 10. (Original) 10. The apparatus of claim 9 further comprising one or
2 more central processing units (CPUs) assignable by said hypervisor to one or more of said
3 partitions, said hypervisor further setting the override bit of one partition when that
4 partition does not have a CPU assigned to it.

1 Claim 11. (Cancelled by this amendment)

1 Claim 12. (Cancelled by this amendment)

1 Claim 13. (Cancelled by this amendment)

1 Claim 14. (Currently Amended) A method for controlling the transfer of data
2 in a data processing system having a processor handling an I/O request in an I/O operation,
3 main storage controlled by the processor for storing data, and one or more I/O devices for
4 sending data to or receiving data from said main storage, said method comprising:
5 _____ registering in a vector mechanism, I/O requests by said devices to send or receive
6 data from said main storage;
7 _____ polling with a dispatcher, said vector mechanism to determine if there is an
8 outstanding I/O request; and



9 sending an immediate interrupt to said processor when an override bit has a first
10 condition for handling an I/O request from said I/O device(s), or polling with said
11 dispatcher, said vector mechanism to determine if there is an outstanding I/O request when
12 said override bit is in a second condition, and

13 ~~The method of claim 13~~ wherein said data processing further includes a Target
14 Delay Interval (TDI) register containing a TDI value for determining when the vector
15 mechanism should not be polled by said dispatcher and an interrupt given to said
16 processor, said method further comprising ~~overriding~~ overriding said TDI value and
17 driving an immediate interrupt to said processor when said ~~override~~ override bit is in its
18 first condition.

1 Claim 15. (Currently Amended) The method of claim ~~13~~ 14 wherein said
2 main storage is divided into multiple partitions, with each partition having a vector
3 mechanism operable to register I/O requests by said devices to send or receive data from
4 that partition of main storage, each partition having an associated override bit for that
5 partition, and said processor is a hypervisor, said method further comprising setting by
6 said hypervisor the override bit for that partition when said hypervisor is to handle an
7 immediate interrupt rather than polling by said dispatcher for that partition.

1 Claim 16. (Original) The method of claim 15 wherein said data processing
2 system further includes one or more central processing units (CPUs) assignable by said
3 hypervisor to one or more of said partitions, said method further comprising setting by
4 said hypervisor, the override bit of one partition when that partition does not have a CPU
5 assigned to it.

1 Claim 17. (Cancelled by this amendment)

1 Claim 18. (Cancelled by this amendment)

1 Claim 19. (Cancelled by this amendment)



1 Claim 20. (Currently Amended) A program product for controlling the
2 transfer of data in a data processing system having a processor handling an I/O request in
3 an I/O operation, main storage controlled by the processor for storing data, and one or
4 more I/O devices for sending data to or receiving data from said main storage, said
5 program product comprising:
6 a computer readable medium having recorded thereon computer readable program
7 code means for performing the method comprising:
8 registering in a vector mechanism, I/O requests by said devices to send or receive
9 data from said main storage;
10 polling with a dispatcher, said vector mechanism to determine if there is an
11 outstanding I/O request; and
12 sending an immediate interrupt to said processor when an override bit has a first
13 condition for handling an I/O request from said I/O device(s), or polling with said
14 dispatcher, said vector mechanism to determine if there is an outstanding I/O request when
15 said override bit is in a second condition, and
16 ~~The program product of claim 19~~ wherein said data processing further includes a
17 Target Delay Interval (TDI) register containing a TDI value for determining when the
18 vector mechanism should not be polled by said dispatcher and an interrupt given to said
19 processor, said method further comprising ~~overriding~~ overriding said TDI value and
20 driving an immediate interrupt to said processor when said ~~override~~ override bit is in its
21 first condition.

1 Claim 21. (Currently Amended) The program product of claim ~~19~~ 20
2 wherein said main storage is divided into multiple partitions, with each partition having a
3 vector mechanism operable to register I/O requests by said devices to send or receive data
4 from that partition of main storage, each partition having an associated override bit for that
5 partition, and said processor is a hypervisor, said method further comprising setting by
6 said hypervisor the override bit for that partition when said hypervisor is to handle an
7 immediate interrupt rather than polling by said dispatcher for that partition.



1 Claim 22. (Original) The program product of claim 21 wherein said data
2 processing system further includes one or more central processing units (CPUs) assignable
3 by said hypervisor to one or more of said partitions, said method further comprising
4 setting by said hypervisor, the override bit of one partition when that partition does not
5 have a CPU assigned to it.

1 Claim 23. (Cancelled by this amendment)